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Guide to CompactPCI Express

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The next generation of CompactPCI is beginning to roll out in the form of CompactPCI Express. This upgraded standard includes substantial performance increases, compatibility with both legacy products and the latest office PC technologies, and a unification of backplane buses into a single bus that supports both CPU-to-I/O and CPU-to-CPU communications.

Historical Perspective

CompactPCI was developed in 1996 as a standard bus structure that combines the cost-effective PC bus architecture (PCI) with the popular Eurocard industrial board form factor. This combination quickly became the world's most popular bus structure for industrial, communications, military and test systems where PCI is used in a rugged form factor. In 2005, the PICMG standards body defined a new CompactPCI specification that incorporates the new PCI Express (PCIe) bus in place of the original PCI bus.

The addition of PCIe to the CompactPCI standard allows CompactPCIe to utilize the latest PC market components; and in turn extends the useful lifespan for the bus architecture for at least the next decade.

Products based on the new standard are now becoming available, with many more product announcements anticipated over the next several months and years.

Benefits of CompactPCIe

CompactPCIe brings several benefits to traditional CompactPCI applications, including:

- **Higher Performance:**
  - Bus transfer speeds increase 10-50X
  - PCIe connections are all point-to-point, eliminating arbitration delays
  - CPU-to-CPU transfers can occur at the full bus bandwidth
    - No need to run relatively slow Ethernet through the backplane
- **Compatibility with legacy boards and chassis**
  - Hybrid systems that include a mix of CompactPCIe as well as legacy CompactPCI slots are easily implemented
  - Since the boards are the same form factor and include the same face plates and other mounting hardware, existing chassis need only upgrade their backplane to be used in CompactPCIe
- **Low costs through access to the latest commodity components**
  - The latest I/O components that include native PCIe interfaces can be easily designed into new CompactPCIe I/O boards

- **New capability to run PCIe over cable**
  - Allows attached PCs to control a CompactPCIe sub-system at full speed and with full S/W transparency
- **Bus Unification, improved multi-processing and fault-tolerance**
  - By incorporating Advanced Switching (ASI) extensions to PCIe, CompactPCIe supports both CPU-to-I/O and CPU-to-CPU communications over the common backplane
  - This provides a cost-effective upgrade path for PICMG 2.16 applications

CompactPCIe Basics

CompactPCIe replaces the P1 and P2 connectors used in CompactPCI with four connectors that provide the new PCIe bus as well as enhanced power capabilities to each board, as shown is figure 1. The bottom connector provides high current connections for incoming power; the second and third connectors provide the PCIe differential pairs for multiple PCIe busses to be routed from each board to the backplane. The top connector provides utility pins for user-defined rear I/O, PXI extensions for instrumentation and power input for the low-cost Type II I/O modules.

System slot boards within CompactPCIe drive either 2 or 4 PCIe buses onto the backplane. This allows the direct connection of up to 4 I/O slots. For larger configurations, a switch is needed to expand the PCIe fan out to additional I/O slots. An 8-port switch board is shown in figure 2.

A bridge board can connect one PCIe port to traditional PCI, enabling hybrid systems that contain a mix of CPCIe and legacy CPCI slots. Figure 3 shows a 6U CompactPCIe backplane that supports this hybrid architecture.

Internal or external CPU – Both are supported

One of the new capabilities of PCIe is the ability to run the bus at full performance with total software transparency over a cable as well as a backplane. For CompactPCI and CompactPCIe systems, this enables system configurations where the CPU element is external from the CompactPCIe system. Figure 4 shows a development system for CompactPCIe that is based on an external PC attached via PCIe over cable.

Deciding whether to have an attached PC versus an internal CPU involves several tradeoffs. Attached PCs are often more robust, offering the latest CPU speeds, memory and peripherals. Embedded PCs have the advantage of eliminating the second chassis, and providing a more consistent level of ruggedness. Often, designers will choose the convenience of an attached PC for development, and then transition to an embedded CPU board for production.

Tree and network topologies

CompactPCIe supports both tree and network topologies. A tree architecture includes one CPU element connected to a number of I/O elements. This is the most cost-effective topology and is suitable for many applications where a single CPU is needed.

CompactPCIe also supports multi-CPU applications. These applications take advantage of the Advanced Switching Interface extensions to PCIe.

ASI within CompactPCIe

Advanced Switching Interface (ASI) is an extension to PCIe that allows CPU-to-CPU communication and dynamic I/O mapping to work on top of the basic PCIe functionality. For multi-CPU systems, this provides a unification of the CPU-to-CPU communications bus and the I/O bus structure. This unification provides dramatic improvements in performance, system cost and fault-tolerance.

Advanced Switching Interface (ASI) is a protocol that resides on top of the basic PCIe packets and adds additional routing information to each packet. This extra protocol allows the PCIe topology to be extended to support full network topologies that include multiple CPUs and dynamically mapable I/O.

Systems based on ASI within CompactPCIe utilize the same CPU and I/O boards as tree architecture systems. A different switch board is needed, however, to provide the PCIe-to-ASI bridges for the CPU boards and the ASI-based switch functionality.

PICMG 2.16 Solution for Multiprocessing

Both CompactPCI and CompactPCIe have built-in flexibility via their P3, P4 and P5 connectors that are available for user defined rear I/O and/or secondary buses or interconnects. Several uses for these connectors have become standardized. One of the most popular is PICMG 2.16 that defines how 1Gb Ethernet can be routed through the P3 connectors to a special 2.16 switch slot. This mechanism allows multiple CPU boards to intercommunicate via the Ethernet in a network topology. “Split backplane” solutions have extended this concept to allow multiple CPU domains (isolated CPU and I/O slots) to be integrated within a single system, with the CPU boards connected by Ethernet routed via 2.16.

ASI as an Upgrade Path for 2.16 Systems

ASI within CompactPCIe provides a particularly attractive upgrade path to 2.16-based systems. The advantages of ASI include 10 – 50X higher performance, lower costs and dynamic I/O mapping.

ASI performance depends on the lane width of the underlying PCIe buses. Typical systems will include two independent x4 PCIe bus interfaces from each CPU board. Each of these interfaces operates at 10Gb per second. Higher performance is achievable by

boards that utilize x8 or x16 interfaces, or from the move to Gen 2 timing, which is expected to become available in late 2007.

Lower costs result from the combination of two buses (PCI and Ethernet in 2.16) into one PCIe bus that performs both functions. CPU boards don't need to drive the extra Ethernet ports into the backplane, and an expensive 2.16 switch board is eliminated. The CompactPCIe with ASI solution does require its own switch board, but this function provides both the I/O board fan-out and multiprocessor switching functions.

Dynamic I/O mapping allows any PCIe I/O function to be mapped to any CPU board, with the mapping changeable on the fly. This capability provides greater hardware configuration flexibility and enhanced fault-tolerance. If a CPU board fails, a different CPU board can be re-mapped to take over control of the I/O boards. This type of capability doesn't exist within 2.16 systems. In those systems, if the controlling CPU board goes down, all the I/O associated with that CPU also goes down.

Conclusions

CompactPCIe provides the advanced features of PCIe in the CompactPCI form factor. In doing so, it extends the useable lifespan of the architecture for at least another decade. The first products based on this new standard are now beginning to appear, and represent the first look into this powerful architecture of the future.

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